ABSTRACT OF THE DISCLOSURE

A single-port hierarchical memory structure including memory modules having memory cells; hierarchically-coupled local and global sense amplifiers; hierarchically-coupled local and global row decoders; and a predecoding circuit coupled with selected global row decoders. The predecoding circuit is disposed to provide predecoding at a speed substantially faster than the predetermined memory access speed of the memory structure, allowing access to a memory cell at least twice during the memory access period, thereby providing dual-port functionality. A WRITE-AFTER-READ operation without a separate, interposed PRECHARGE cycle, is completed within one memory access cycle of the hierarchical memory structure. The method includes locally selecting the first memory location of a first datum; locally sensing the first datum (i.e., the READ operation); globally selecting, the second memory location; concurrently with the globally selecting, globally sensing the first datum at the first memory location; outputting the first data subsequent to the globally sensing; inputting the second datum substantially immediately subsequent to the outputting the first datum; locally selecting the second memory location; and storing the second datum (i.e., WRITE operation). Also, a WRITE-AFTER-WRITE operation similarly is accomplished by interposing a PRECHARGE operation between subsequent WRITE operations. A redundant group of memory cells, and techniques for assigning them to a memory location in a "FAULT" condition, also are provided.